Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended): A method for manufacturing a semiconductor power device, comprising:

identifying an active region on a semiconductor die, the active region having a central portion and a first peripheral portion disposed about a periphery of said central portion;

identifying a first region in said central portion of said active region;

identifying a second region in said first peripheral portion of said active region;

~~identifying a third region in said active region;~~

~~providing~~ fabricating active cells in accordance with a first cell design ~~by which active cells~~ in said first region ~~will be fabricated~~;

~~providing~~ fabricating active cells in accordance with a second cell design ~~by which active cells~~ in said second region, wherein a combined current density of said active cells fabricated according to said second cell design is greater than a combined current density of said active cells fabricated according to said first cell design during operation of said active cells ~~will be fabricated; and~~

~~providing a third cell design by which active cells in said third region will be fabricated,~~

~~wherein first active cells fabricated according to said first cell design are different from second active cells fabricated according to said second cell design,~~

~~wherein third active cells fabricated according to said third cell design are different from said first active cells and from said second active cells~~.

2. (Original): The method of claim 1 wherein said first cell design and said second cell design include cell dimensions such that a cell density of said first region is different from that of said second region.

3. (Original): The method of claim 1 wherein said first cell design includes at least one physical dimension different from that included in said second cell design.

4. (Original): The method of claim 3 wherein said physical dimension includes a channel width.

5. (Original): The method of claim 4 wherein said physical dimension includes a cell die area.

6. (Original): The method of claim 1 wherein said first cell design includes a material composition for cells that is different from that of said second cell design.

7. (Original): The method of claim 1 wherein said first cell design differs from said second cell design with respect to current density.

8. (Original): The method of claim 1 wherein said first cell design differs from said second cell design with respect to source resistance.

9. (Original): The method of claim 1 wherein said first cell design differs from said second cell design with respect to transconductance.

10. (Original): The method of claim 1 wherein said first cell design differs from said second cell design with respect to gain.

11. (Original): The method of claim 1 wherein said first cell design differs from said second cell design with respect to threshold voltage.

12. (Original): The method of claim 1 wherein said first cell design and said second cell design are field effect transistors.

13. (Original): The method of claim 1 wherein said first cell design and said second cell design are memory cells.

14. (Previously presented): A semiconductor power device fabricated in accordance with the method of claim 1.

15. (New): The method of claim 1 further comprising disposing a plurality of terminating cells about a periphery of said active region.

16. (New): The method of claim 1 wherein said active region further has a second peripheral portion disposed about a peripheral region of said first peripheral portion, the method further comprising identifying a third region in said second peripheral portion and fabricating active cells in accordance with a third cell design in said third region, wherein during operation of said active cells a combined current density of said active cells fabricated according to said third cell design is greater than both said combined current density of said active cells fabricated according to said first cell design and said combined current density of said active cells fabricated according to said second cell design.

17. (New): A method for manufacturing a semiconductor power device, comprising:

identifying an active region on a semiconductor die;

identifying a first region in said active region;

identifying a second region in said active region;

identifying a third region in said active region;

providing a first cell design by which active cells in said first region will be fabricated;

providing a second cell design by which active cells in said second region will be fabricated; and

providing a third cell design by which active cells in said third region will be fabricated,

wherein first active cells fabricated according to said first cell design are different from second active cells fabricated according to said second cell design,

wherein third active cells fabricated according to said third cell design are different from said first active cells and from said second active cells,

wherein said first cell design and said second cell design are memory cells.